



Attorney Docket No.:AMD-C553397.DIV

2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the U.S. Patent and Trademark Office, Washington, D.C., 20231, on the below date of deposit.			
Date of Deposit:	9/3/02	Name of Person Making the Deposit:	Kerry Erin Kelly
		Signature of the Person Making the Deposit:	<i>Kerry Erin Kelly</i>

In re Application of: Liu et al

Serial No.: 09/629,780

Examiner: Pizarro-Crespo. M.

Filed: 7/31/00

Art Unit: 2814

For: TRENCHED GATE NON-VOLATILE SEMICONDUCTOR METHOD WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE TRENCH BY SIDEWALL DOPING

Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED
SEP 16 2002
TECHNOLOGY CENTER-2800

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

☒ Transmitted herewith is a response to an office action for the above identified patent application
(10 sheets)

Transmitted herewith are sheets of substitute formal drawings.
Other:

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) ☐ Applicant petitions for an extension of time under 37 C.F.R. 1.136
(fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
<input type="checkbox"/> one month	\$110.00
<input type="checkbox"/> two months	\$400.00
<input type="checkbox"/> three months	\$920.00
<input type="checkbox"/> four months	\$1,960.00

Fee \$

If an additional extension of time is required, please consider this a petition therefor.

(b) ☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	4	- 20 =	0	x \$18.00	\$0.00
Independent Claims	1	- 3 =	0	x \$80.00	\$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				\$260.00	
Total Fees					\$0.00

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:
- ☒ The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.
A duplicate copy of this authorization is enclosed.

- ☐ A check in the amount of \$
- ☐ Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: September 3, 2002

By: Jose S. Garcia
Jose S. Garcia
Reg. No.43,628



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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SEP 16 2002
TECHNOLOGY CENTER 2800

In RE Application Of: Liu et al.

Serial No. : 09/629,780

Group Art Unit: 2814

Filed : July 31, 2000

Examiner: PIZARRO-CRESPO, M.

For : TRENCHED GATE NON-VOLATILE SEMICONDUCTOR METHOD
WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE
TRENCH BY SIDEWALL DOPINGS

AMENDMENT AND RESPONSE

#9/Amend B
Aranda
9/24/02

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed 6/05/2002, please enter and
consider the following amendments and arguments for the above captioned
patent application.

IN THE CLAIMS

Please amend Claims 16 and 19 as follows:

16. (Once amended) A method for fabricating a semiconductor device with
a ~~trenched gate~~ comprising:
etching a trench having substantially upright vertical sidewalls and a
bottom surface in a semiconductor substrate;
forming a trench-to-gate insulating layer inside the trench, wherein the
trench-to-gate insulating layer comprises a trench gate dielectric spacer formed